Printed Pages : 3

EEC-302

(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : **131305**

Roll No. | | | | | | | | | | |

B. Tech.

(SEM. III) (ODD SEM.) THEORY EXAMINATION, 2014-15

DIGITAL ELECTRONICS

Time : **3** Hours] [Total Marks : **100**

Note : Attempt ALL questions.

1 Answer any **four** parts : **5×4=20**

(a) Represent the decimal number 6208 (i) in2,4,2,1 code, (ii) in BCD and (iii) as a binary number.

(b) Define parity codes. Design odd parity generator and parity checker for three bit codes data.

(c) Construct 16 × 1 Multiplexer with the help of 4 × 1 Multiplexer.

(d) Compute M-N and N-M using 1's compliment and 2's compliment methods. Where, M=110100 and N=10101.

(e) Implement Boolean function of Ex-NOR with the help of (i) using NAND Gates only and (ii) using NOR Gates only.

(f) Simplify using Karnaugh map the following Boolean Function

$F(w,x,y,z)=\sum(1,5,7,10,15)$

$D(w,x,y,z)=\sum(3,2,6)$

2 Answer any **four** parts : **5×4=20**

(a) Implement a full subtractor with two half subtractors.

(b) Design and explain the logic and circuit of 4 bit magnitude comparator.

(c) Design and explain the logic and circuit of 4-bit by 3-bit binary multiplier.

(d) Construct a 5×32 decoder with 3x8 decoders and 2×4 decoder.

(e) Implement the following Boolean function with the help of 4×1 multiplexer

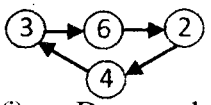
$F(x,y,z)=\sum(1,2,6,7)$

(f) Design and explain the logic and circuit of BCD Adder.

3 Answer any **two** parts : **10×2=20**

(a) Design a modulo-14 ripple counter. Give its waveforms displaying output states.

(b) Design a synchronous counter using JK Flip Flop which can count the following cycle. Also draw the bush diagram.



(c) (i) Draw and explain the circuit of bidirectional shift register with parallel load.

(ii) Draw and explain the circuit of Ring Counter and Johnson Counter. Write the output states of these counters.

4 Answer any **two** parts : **10×2=20**

(a) Draw and explain the circuit of a memory binary cell. Using this binary cell draw and explain the circuit of 8×5 RAM.

(b) Explain PROM, PLA and PAL. Implement the following Boolean functions with a PLA. $F_1(x,y,z)=\sum(0,2,3,4)$; $F_2(x,y,z)=\sum(2,4,6,7)$

(c) Explain ASM Chart. Describe the ASM chart and control logic of Binary Multiplier.

5 Answer any **two** parts : **10×2=20**

(a) An asynchronous sequential circuit is decribed the excitation and output functions as given below.

$Y_1=x_1x_2+x_1y_2'+x_2'y_1$; $Y_2=x_2+x_1y_1'y_2+x_1'y_1$; $z=x_2+y_1$

(i) Draw the logic diagram of the circuit (ii) Derive the transition and output map (iii) Obtain a flow table of the circuit.

(b) Analyze SR latch with NOR gates. The Boolean functions for the inputs of an SR latch are

$S= x_1' x_2'x_3+x_1x_2x_3$

$R= x_1 x_2'+x_2x_3'$

Obtain the circuit diagram using a minimum number of NAND Gates.

(c) Obtain a binary state assignment for the reduced flow table shown below. Avoid critical race conditions. Also obtain the logic diagram of the circuit using NAND latches and gates.

	x_1x_2 = 00	01	11	10
a	(a), 0	(a), 1	b, -	d, -
b	a, -	(b), 0	(b), 0	c, -
c	a, -	-, -	d, -	(c), 0
d	a, -	a, -	(d), 1	(d), 1