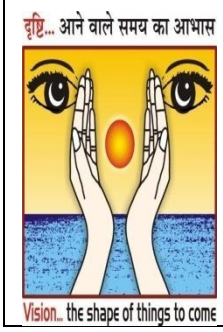
VISION INSTITUTE OF TECHNOLOGY, KANPUR

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING



Sub code & Name: Digital Electronics

Semester & Year : 4th 2nd year

Branch :ECE

Faculty Name : Mr. Satyam Yadav

Unit -1

1. State de-morgan`s theorem and mention its use?
2. Implement truth table of Ex OR gate?
3. Express the function Y= A+ BC into canonical POS form.
4. Find the 2`s complement of given function
   a. 1000 b. 10010
5. Convert

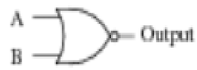
   $(256)_{10} \rightarrow (\ldots\ldots)_2$
   $(35)_{10} \rightarrow (\ldots\ldots)_2$

6. Simplify the following switching function using Karnaugh map(K-map) method and realize expression using gates
   $F(A,B,C,D) = \sum(0,3,5,7,8,9,10,12,15)$
7. Implement full adder circuit using Half Adders and make truth table?
8. Define the logic output ?
9. Define min-term and max-term?
10. What are universal gate why these gates are called universal gates?
11. Explain binary half adder and draw logic diagram?
12. What is multiplexer? what are the use of select line?
13. Identify each of these logic gates and complete truth table?
14.

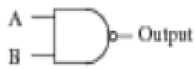
A	B	Output
0	0	
0	1	
1	0	
1	1	

A	B	Output
0	0	
0	1	
1	0	
1	1	

A	B	Output
0	0	
0	1	
1	0	
1	1	



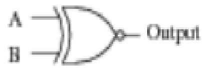
A	B	Output
0	0	
0	1	
1	0	
1	1	



A	B	Output
0	0	
0	1	
1	0	
1	1	

A	B	Output
0	0	
0	1	
1	0	
1	1	

A	B	Output
0	0	
0	1	
1	0	
1	1	



A	B	Output
0	0	
0	1	
1	0	
1	1	

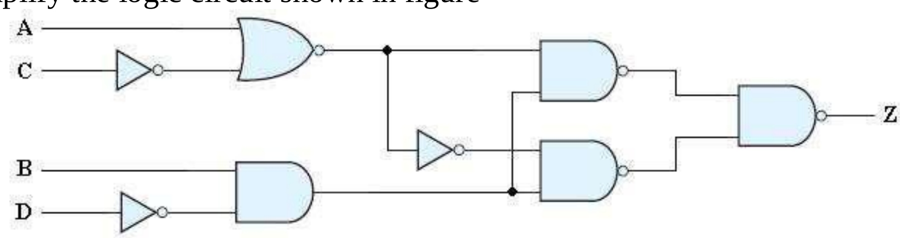
A	Output
0	
1	

15.

Unit -2

1. Simplify the following function using K – map, f=ABCD+AB’C’D’+AB’C+AB & realize the SOP using only NAND gates and POS using only NOR gates (12)

   ii). Simplify the logic circuit shown in figure (4)



2. a). i). Minimize the term using Quine McCluskey method & verify the result using K-map method πM(0,1,4,11,13,15)+ πd(5,7,8). (10)

   ii). Explain the operation of 3 input TTL NAND gate with required diagram & truth table. (6)

3. a). i). Using K-map method, Simplify the following Boolean function and obtain
   (a) minimal SOP and
   (b) minimal POS expression & realize using only NAND and NOR gates
   $F=\sum_m(0,2,3,6,7) + d(8,10,11,15)$ (10)
   ii). Draw the circuits of 2 input NAND & 2 input NOR gate using CMOS (6)

4. a). i). Using Quine McCluskey method Simplify the Boolean expression
   $F(v,w,x,y,z) = \sum (4,5,9,11,12,14,15,27,30) + \sum ø(1,17,25,26,31)$ (10)
   ii). Explain the working of a basic totem-pole TTL 2 input NAND gate. (6)

5. a).i).Find a minimal SOP representation for $f(A,B,C,D,E) = \sum_m(1,4,6,10,20,22,24,26) + d(0,11,16,27)$ using K-map method. Draw the circuit of the minimal expression using only NAND. (12)
   ii). Obtain 3 level NOR – NOR implementation of f = [ab + cd] ef (4)

6. Minimize the term using Quine McCluskey method & verify the result using K-map method $\Pi_M(1,4,5,9,12,13,14) \cdot \Pi_d(8,10,11,15)$. (16)
7. Find a minimal SOP representation for $f(A,B,C,D,E)=\sum_m(1,4,6,10,20,22,24,26)+ d(0,11,16,27)$ using K-map method. Draw the circuit of the minimal expression using only NAND. (16)
8. (i)Given Y (A, B, C, D) = $\prod_M$ (0, 1, 3, 5, 6, 7, 10, 14, 15), draw the K-map and obtain the simplified expression. Realize the minimum expression using basic gates. (8)
   (ii) Prove by perfect induction (8)
   (i). A+AB = A
   (ii) A(A+B) = A
   (iii) A+A'B = A+B and
   (iv) A(A'+B) =AB

Unit-3

1. Draw the block schematic of Magnitude comparator and explain its operation
2. Draw & explain the block diagram of a 4-bit parallel adder / Subtractor
3. Design & implement the conversion circuits for BCD to Excess – 3 code.
4. (i) Design a BCD to Gray code converter. Uses don't care.
   (ii) Implement full subtractor using Demultiplexer.
5. Design an Excess – 3 to BCD code converter. Uses don't care
6. (i). Implement full adder using decoder.
   (ii).Realize $F(w, x, y, z)= \Sigma (1,4,6,7,8,9,10,11,15)$ using 8 to 1 Mux
7. Explain the operation of carry look ahead adder with neat diagram
8. (i). Draw and explain the BCD adder circuit.
   (ii). Design a seven segment decoder circuit to display the numbers from 0 to 3.

9. (i).Design & explain the working of Gray to BCD converter. (ii).Explain even parity checker and generator.

10. (i).Draw the logic diagram of BCD to Decimal decoder and explain its operations.